CMOS Static RAM 256K (32K x 8-Bit)

IDT71256S
IDT71256L

Features

- **High-speed address/chip select time**
  - *Military: 25/35/45/55/70/85/100ns (max.)*
  - *Industrial: 25/35ns (max.)*
  - *Commercial: 20/25/35ns (max.) low power only*
- **Low-power operation**
- **Battery Backup operation – 2V data retention**
- **Produced with advanced high-performance CMOS technology**
- **Input and output directly TTL-compatible**
- **Available in standard 28-pin (300 or 600 mil) ceramic DIP, 28-pin (600 mil) plastic DIP, 28-pin (300 mil) SOJ and 32-pin LCC**
- **Military product compliant to MIL-STD-883, Class B**

Description

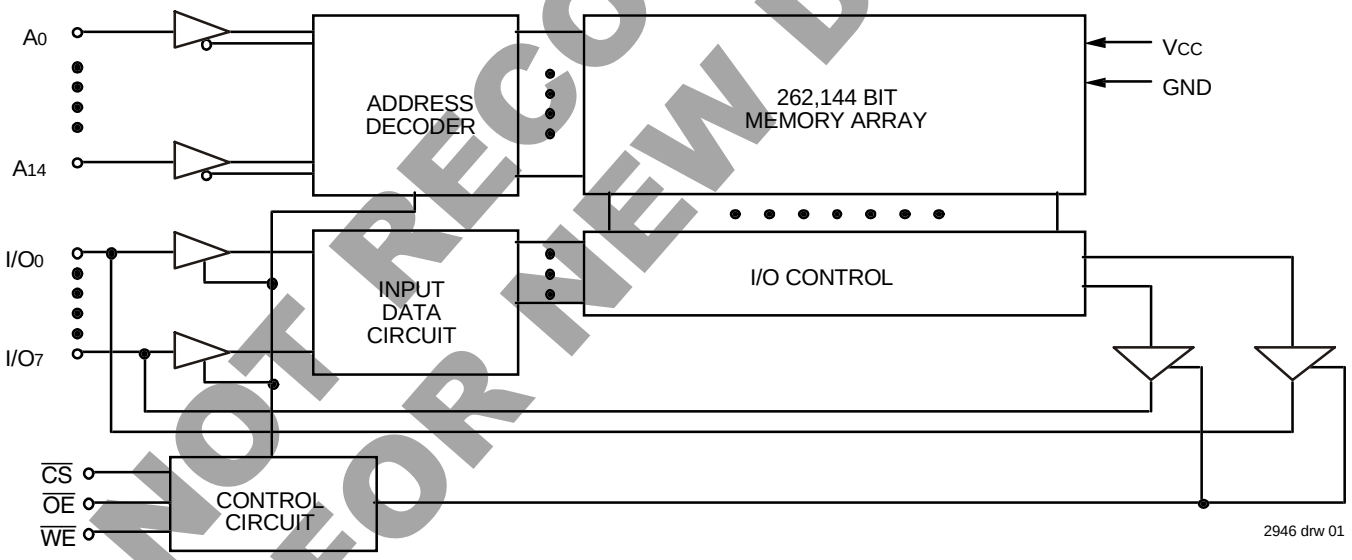
The IDT 71256 is a 262,144-bit high-speed static RAM organized as 32K x 8. It is fabricated using IDT's high-performance, high-reliability CMOS technology.

Address access times as fast as 20ns are available with power consumption of only 350mW (typ.). The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes HIGH, the circuit will automatically go to and remain in, a low-power standby mode as long as $\overline{CS}$ remains HIGH. In the full standby mode, the low-power device consumes less than 15µW, typically. This capability provides significant system level power and cooling savings. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 5µW when operating off a 2V battery.

The IDT71256 is packaged in a 28-pin (300 or 600 mil) ceramic DIP, a 28-pin 300 mil SOJ, a 28-pin (600 mil) plastic DIP, and a 32-pin LCC providing high board level packing densities.

The IDT71256 military RAM is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

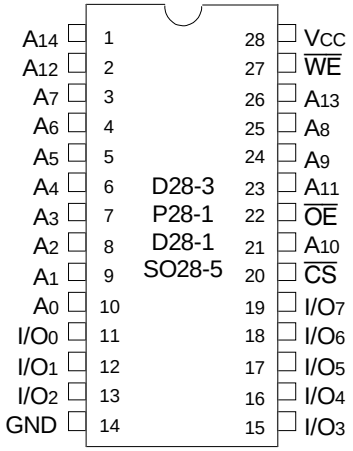
Functional Block Diagram



2946 drw 01

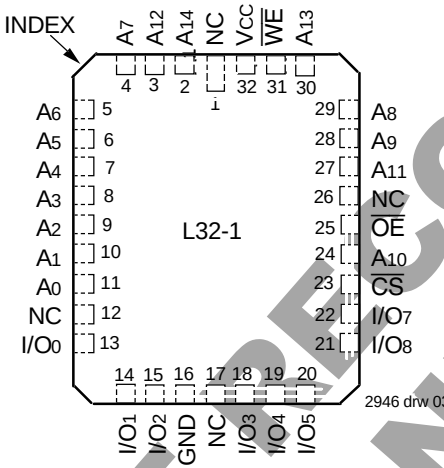
AUGUST 2000

Pin Configurations



2946 drw 02

DIP/SOJ
Top View



2946 drw 03

32-Pin LCC
Top View

Truth Table[1]

WE	CS	OE	I/O	Function
X	H	X	High-Z	Standby (I_{SB})
X	V_{HC}	X	High-Z	Standby (I_{SB1})
H	L	H	High-Z	Output Disabled
H	L	L	D_{OUT}	Read Data
L	L	X	D_{IN}	Write Data

2946 tbl 02

NOTE:
1. H = V_{IH}, L = V_{IL}, X = Don't care.

Absolute Maximum Ratings[1]

Symbol	Rating	Com'l.	Ind.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-40 to +85	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	50	mA

2946 tbl 03

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Pin Descriptions

Name	Description
A_0 - A_{14}	Address Inputs
I/O_0 - I/O_7	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
GND	Ground
V_{CC}	Power

2946 tbl 01

Capacitance (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	11	pF

2946 tbl 04

NOTE:
1. This parameter is determined by device characterization, but is not production tested.

Recommended Operating Temperature and Supply Voltage

Grade	Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5V ± 10%
Industrial	-40°C to +85°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2946 tbl 05

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

2946 tbl 06

NOTE:
1. V_{IL} (min.) = –3.0V for pulse width less than 20ns, once per cycle.

DC Electrical Characteristics(1,2) (V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	71256S/L20		71256S/L25		71256S/L35		71256S/L45		Unit
			Com'l.	Mil.	Com'l & Ind	Mil.	Com'l. & Ind	Mil.	Com'l.	Mil.	
I_{CC}	Dynamic Operating Current $\overline{CS} \leq V_{IL}$, Outputs Open V_{CC} = Max., f_{MAX}(2)	S	—	—	—	150	—	140	—	135	mA
		L	135	—	115	130	105	120	—	115	
I_{SB}	Standby Power Supply Current (TTL Level), $\overline{CS} \geq V_{IH}$, V_{CC} = Max., Outputs Open, f = f_{MAX}(2)	S	—	—	—	20	—	20	—	20	mA
		L	3	—	3	3	3	3	—	3	
I_{SB1}	Full Standby Power Supply Current (CMOS Level), $\overline{CS} \geq V_{HC}$, V_{CC} = Max., f = 0	S	—	—	—	20	—	20	—	20	mA
		L	0.4	—	0.4	1.5	0.4	1.5	—	1.5	

2946 tbl 07

Symbol	Parameter	Power	71256S/L55	71256S/L70	71256S/L85	71256S/L100	Unit
			Mil.	Mil.	Mil.	Mil.	
I_{CC}	Dynamic Operating Current $\overline{CS} \leq V_{IL}$, Outputs Open V_{CC} = Max., f_{MAX}(2)	S	135	135	135	135	mA
		L	115	115	115	115	
I_{SB}	Standby Power Supply Current (TTL Level), $\overline{CS} \geq V_{IH}$, V_{CC} = Max., Outputs Open, f = f_{MAX}(2)	S	20	20	20	20	mA
		L	3	3	3	3	
I_{SB1}	Full Standby Power Supply Current (CMOS Level), $\overline{CS} \geq V_{HC}$, V_{CC} = Max., f = 0	S	20	20	20	20	mA
		L	1.5	1.5	1.5	1.5	

2946 tbl 08

NOTES:
1. All values are maximum guaranteed values.
2. f_{MAX} = 1/t_{RC}, all address inputs are cycling at f_{MAX}; f = 0 means no address pins are cycling.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2946 tbl 09

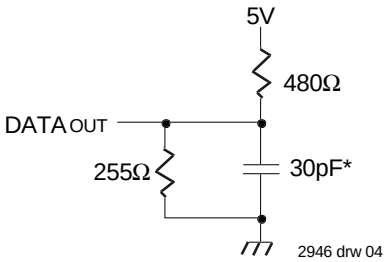


Figure 1. AC Test Load

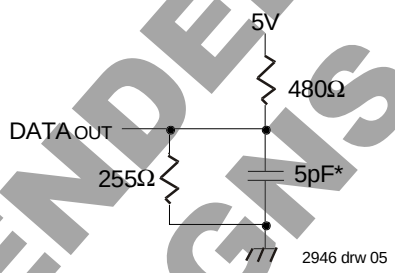


Figure 2. AC Test Load (for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, and t_{WHZ})

*Includes scope and jig capacitances

DC Electrical Characteristics (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions		IDT71256S Min.	IDT71256S Typ.	IDT71256S Max.	IDT71256L Min.	IDT71256L Typ.	IDT71256L Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL. COM'L & IND.	— —	— —	10 5	— —	— —	5 2	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL. COM'L & IND.	— —	— —	10 5	— —	— —	5 2	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.		—	—	0.4	—	—	0.4	V
		I_{OL} = 10mA, V_{CC} = Min.		—	—	0.5	—	—	0.5	
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	—	—	2.4	—	—	V

2946 tbl 10

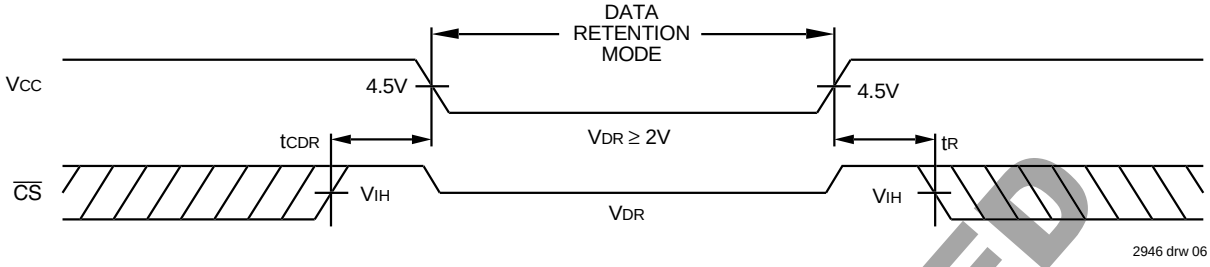
Data Retention Characteristics Over All Temperature Ranges
(L Version Only) (V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Test Condition		Min.	Typ.(1) Vcc @ 2.0V	Typ.(1) Vcc @ 3.0V	Max. Vcc @ 2.0V	Max. Vcc @ 3.0V	Unit
V_{DR}	V_{CC} for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS}$ ≥ V_{HC}	MIL. COM'L. & IND.	— —	— —	— —	500 120	800 200	µA
t_{CDR}	Chip Deselect to Data Retention Time			0	—	—	—	—	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	—	—	—	—	ns

2946 tbl 11

NOTES:
1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed by device characterization, but is not production tested.

Low Vcc Data Retention Waveform



2946 drw 06

AC Electrical Characteristics (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71256L20(1)		71256S25 71256L25		71256S35 71256L35		71256S45(3) 71256L45(3)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	20	—	25	—	35	—	45	—	ns
t_{AA}	Address Access Time	—	20	—	25	—	35	—	45	ns
t_{ACS}	Chip Select Access Time	—	20	—	25	—	35	—	45	ns
t_{CLZ}(2)	Chip Select to Output in Low-Z	5	—	5	—	5	—	5	—	ns
t_{CHZ}(2)	Chip Deselect to Output in High-Z	—	10	—	11	—	15	—	20	ns
t_{OE}	Output Enable to Output Valid	—	10	—	11	—	15	—	20	ns
t_{OLZ}(2)	Output Enable to Output in Low-Z	2	—	2	—	2	—	0	—	ns
t_{OHZ}(2)	Output Disable to Output in High-Z	2	8	2	10	2	15	—	20	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
Write Cycle										
t_{WC}	Write Cycle Time	20	—	25	—	35	—	45	—	ns
t_{CW}	Chip Select to End-of-Write	15	—	20	—	30	—	40	—	ns
t_{AW}	Address Valid to End-of-Write	15	—	20	—	30	—	40	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	15	—	20	—	30	—	35	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{DW}	Data to Write Time Overlap	11	—	13	—	15	—	20	—	ns
t_{WHZ}(2)	Write Enable to Output in High-Z	—	10	—	11	—	15	—	20	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	0	—	ns
t_{OW}(2)	Output Active from End-of-Write	5	—	5	—	5	—	5	—	ns

2946 tbl 12

NOTES:
1. 0° to +70°C temperature range only.
2. This parameter is guaranteed by device characterization, but is not production tested.
3. –55°C to +125°C temperature range only.

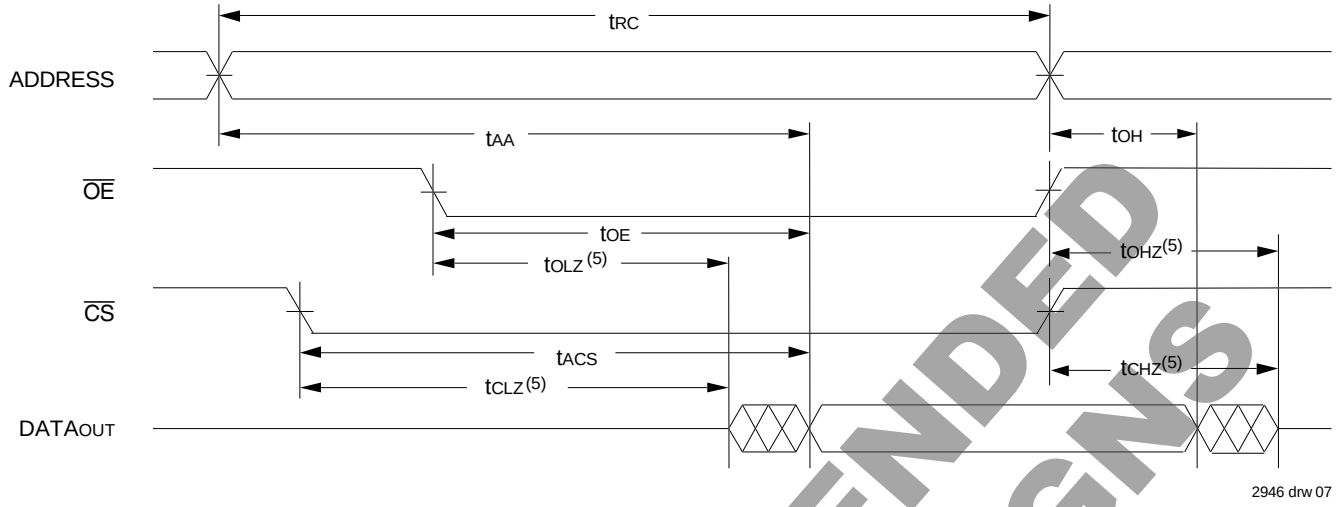
AC Electrical Characteristics (Vcc = 5.0V ± 10%, Military Temperature Ranges)

Symbol	Parameter	71256S55[1] 71256L55[1]		71256S70[1] 71256L70[1]		71256S85[1] 71256L85[1]		71256S100[1] 71256L100[1]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	55	—	70	—	85	—	100	—	ns
t_{AA}	Address Access Time	—	55	—	70	—	85	—	100	ns
t_{ACS}	Chip Select Access Time	—	55	—	70	—	85	—	100	ns
t_{CLZ}[2]	Chip Select to Output in Low-Z	5	—	5	—	5	—	5	—	ns
t_{CHZ}[2]	Chip Deselect to Output in High-Z	—	25	—	30	—	35	—	40	ns
t_{OE}	Output Enable to Output Valid	—	25	—	30	—	35	—	40	ns
t_{OLZ}[2]	Output Enable to Output in Low-Z	0	—	0	—	0	—	0	—	ns
t_{OHZ}[2]	Output Disable to Output in High-Z	0	25	0	30	—	35	—	40	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
Write Cycle										
t_{WC}	Write Cycle Time	55	—	70	—	85	—	100	—	ns
t_{CW}	Chip Select to End-of-Write	50	—	60	—	70	—	80	—	ns
t_{AW}	Address Valid to End-of-Write	50	—	60	—	70	—	80	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	40	—	45	—	50	—	55	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{DW}	Data to Write Time Overlap	25	—	30	—	35	—	40	—	ns
t_{WHZ}[2]	Write Enable to Output in High-Z	—	25	—	30	—	35	—	40	ns
t_{DH}	Data Hold from Write Time ($\overline{WE}$)	0	—	0	—	0	—	0	—	ns
t_{OW}[2]	Output Active from End-of-Write	5	—	5	—	5	—	5	—	ns

2946 tbl 13

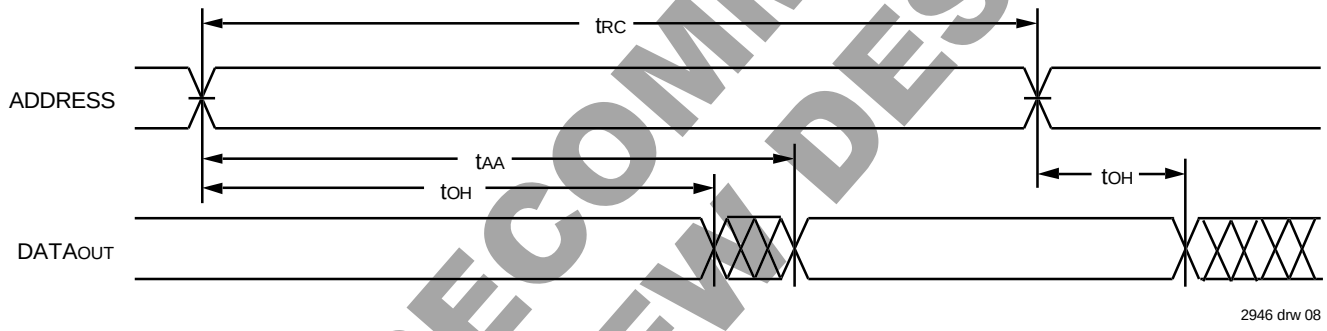
NOTES:
1. -55° to +125°C temperature range only.
2. This parameter is guaranteed by device characterization, but is not production tested.

Timing Waveform of Read Cycle No. 1(1)



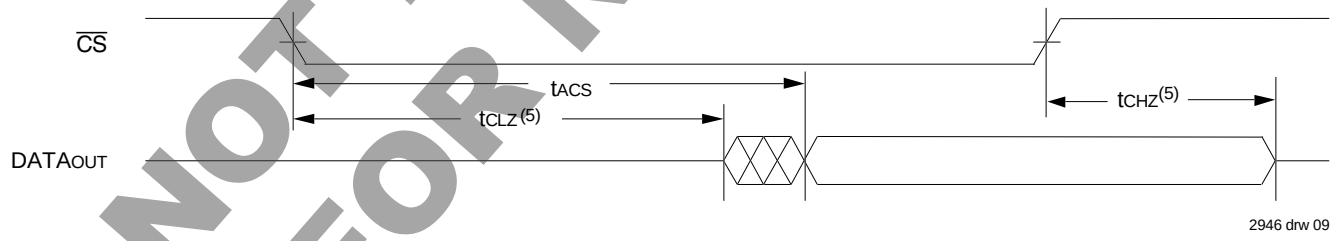
2946 drw 07

Timing Waveform of Read Cycle No. 2(1,2,4)



2946 drw 08

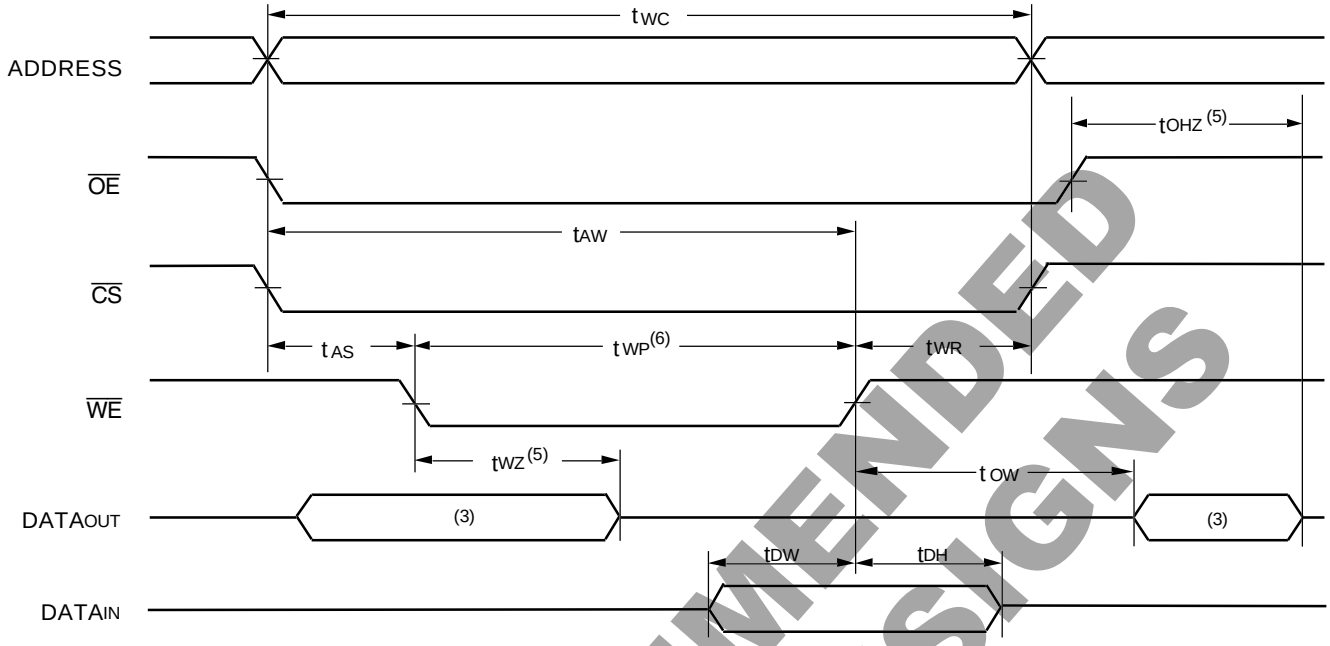
Timing Waveform of Read Cycle No. 2(1,3,4)



2946 drw 09

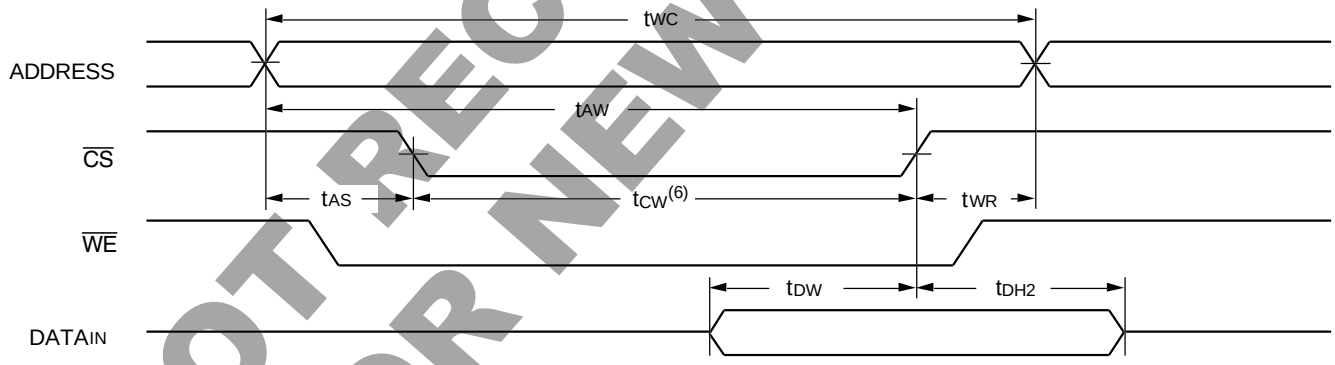
NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ is LOW.
3. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
4. $\overline{OE}$ is LOW.
5. Transition is measured ±200mV from steady state.

Timing Waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled Timing)(1,2,4,6)



2946 drw 10

Timing Waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled Timing)(1,2,4)

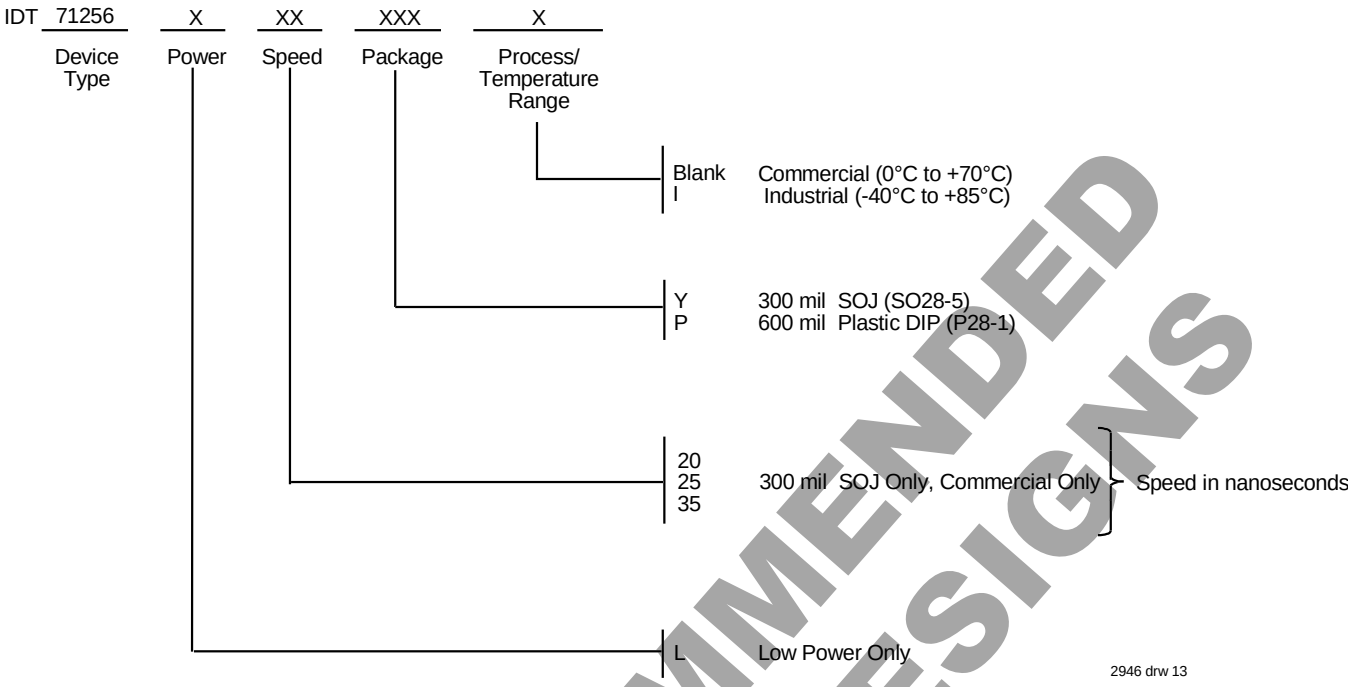


2946 drw 11

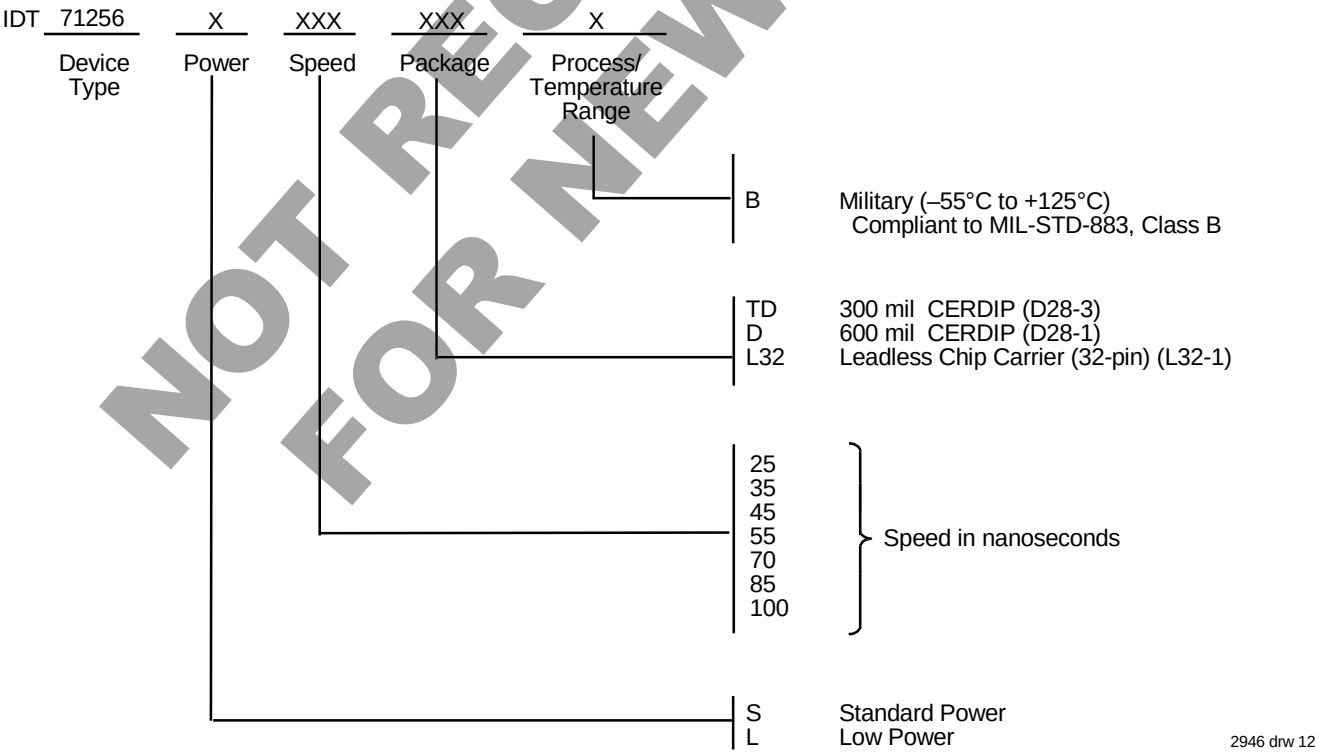
NOTES:

1. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
3. During this period, I/O pins are in the output state so that the input signals must not be applied.
4. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
5. Transition is measured ±200mV from steady state.
6. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} +t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse width can be as short as the specified t_{WP}. For a CS controlled write cycle, $\overline{OE}$ may be LOW with no degradation to t_{CW}.

Ordering Information — Commercial & Industrial



Ordering Information — Military



Datasheet Document History

11/4/99		Updated to new format
	Pp. 1–5, 9	Added Industrial Temperature Range offerings
	Pg. 1	Removed 30, 120, and 150ns military and 45ns commercial speed grade offerings.
	Pg. 2	Removed P28-2 package from DIP/SOJ Top View
	Pg. 3	Removed 30ns and 45ns (Commercial only) speed grade offerings from DC Electrical table Revised notes and footnotes
	Pg. 5	Removed 30ns speed grade offering from AC Electrical table Revised notes and footnotes
	Pg. 6	Expressed Military Temperature range on AC Electrical table Revised notes and footnotes
	Pg. 8	Removed Note 1 and renumbered notes and footnotes
	Pg. 9	Revised Ordering Information and presented by temperature range offering
	Pg. 10	Added Datasheet Document History
08/09/00		Not recommended for new designs

CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015 or 408-727-6116
fax:408-492-8674
www.idt.com

for Tech Support:
sramhelp@idt.com
800 544-7726, x4033